

Fig. 1A

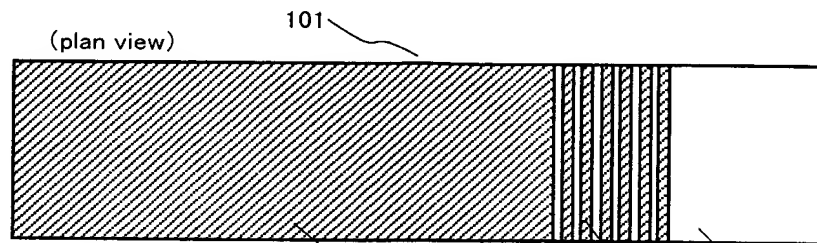


Fig. 1B

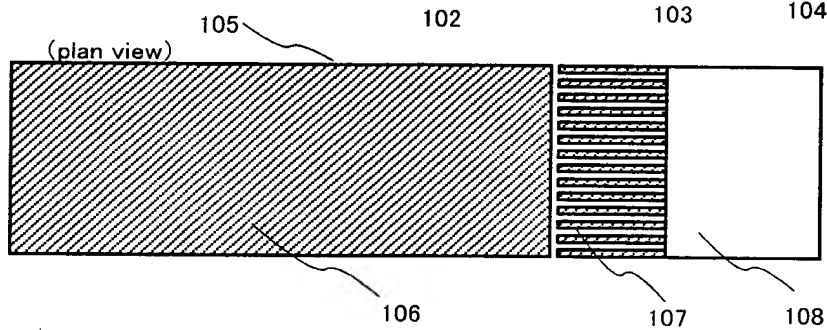


Fig. 1C

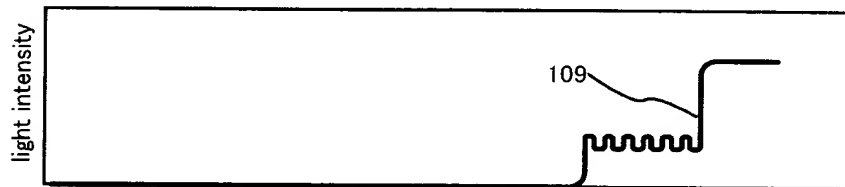


Fig. 1D

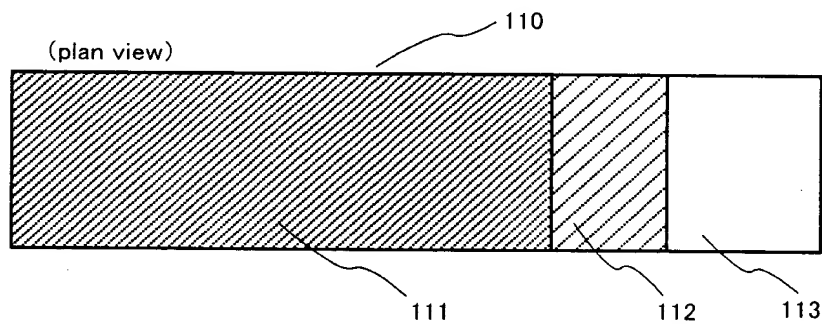


Fig. 1E



Fig. 2A

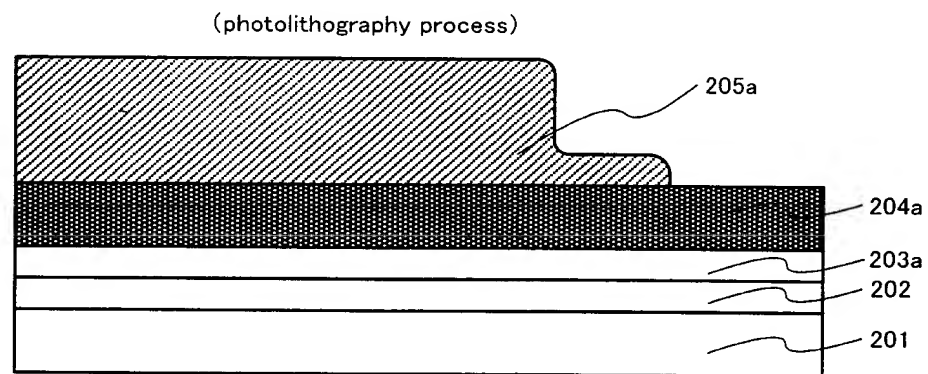


Fig. 2B

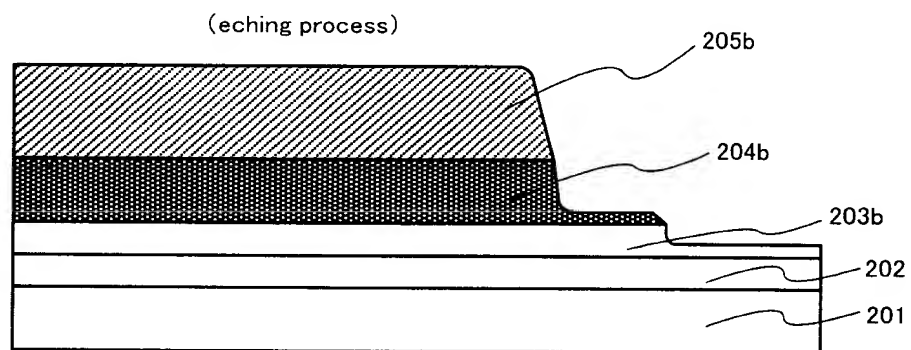


Fig. 2C

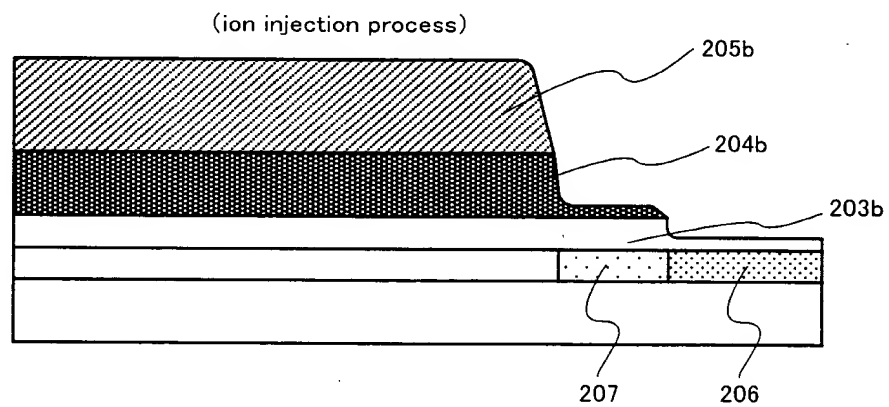


Fig. 3A

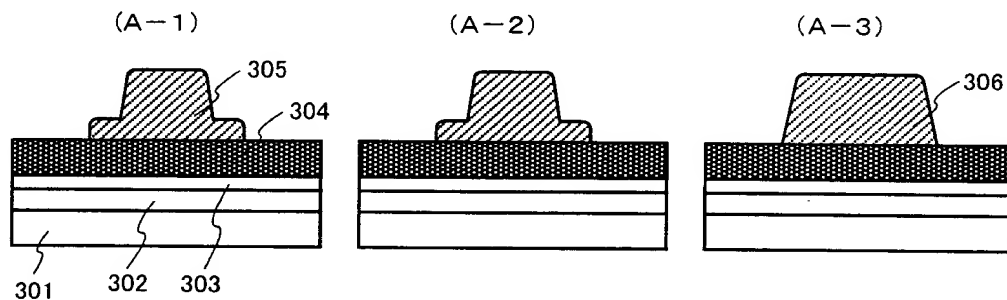


Fig. 3B

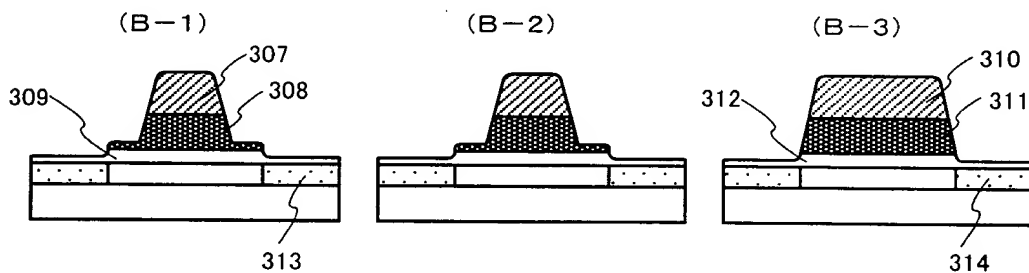


Fig. 3C

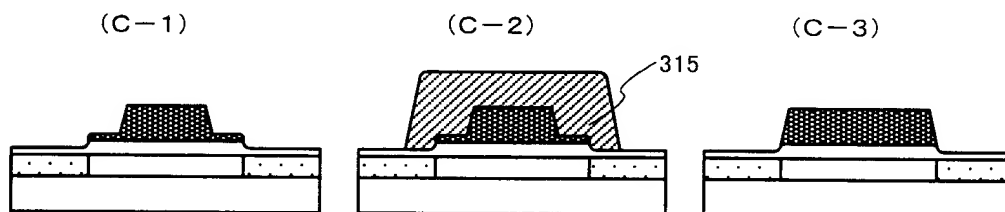
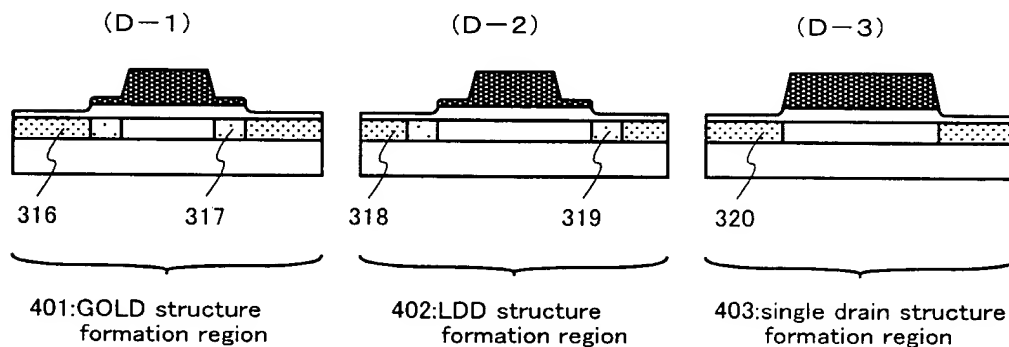


Fig. 3D



506: shift register circuit (GOLD structure)
507: level shifter circuit (GOLD structure)
508: buffer circuit (GOLD structure)

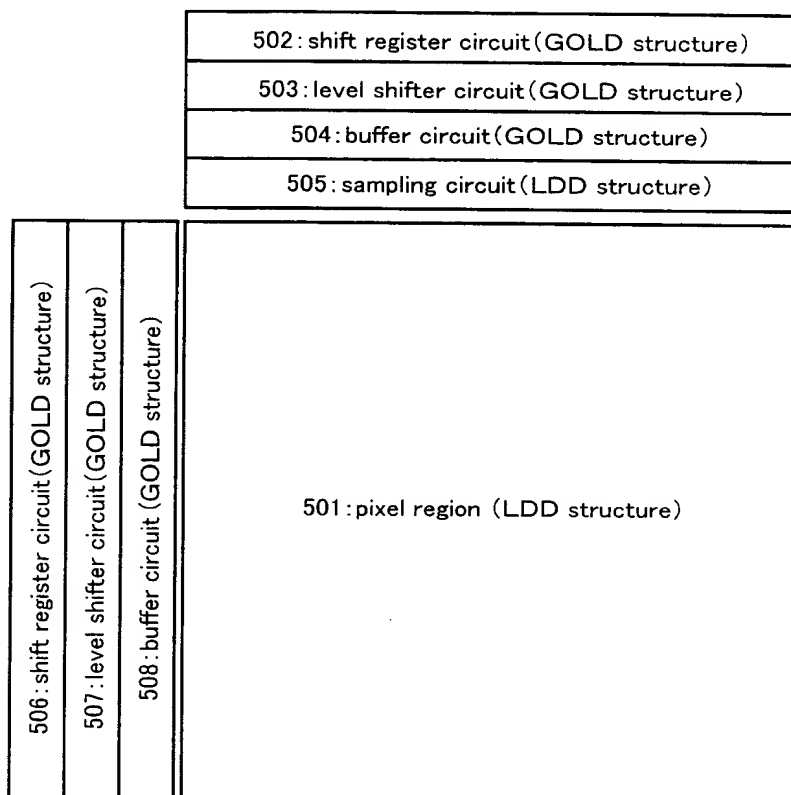


Fig. 4

Fig. 5A

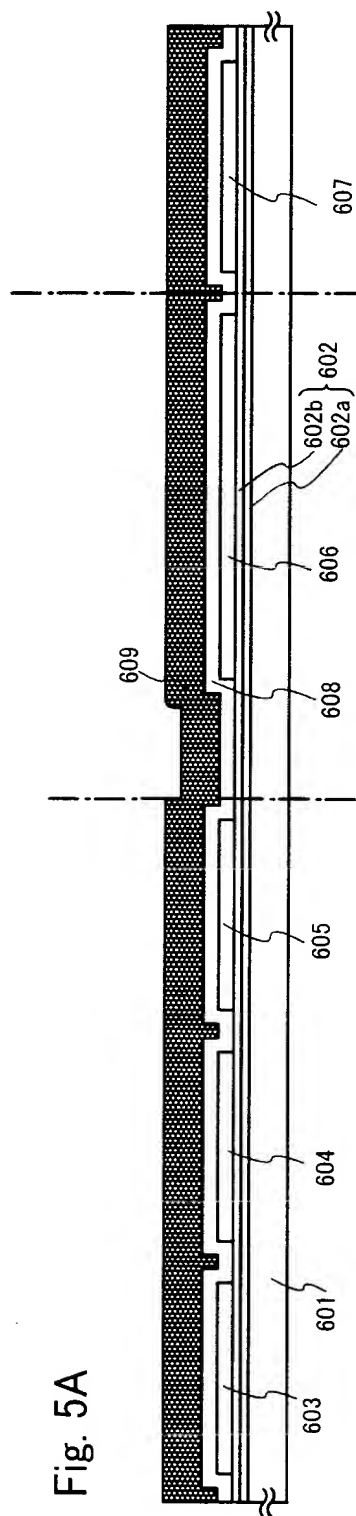


Fig. 5B

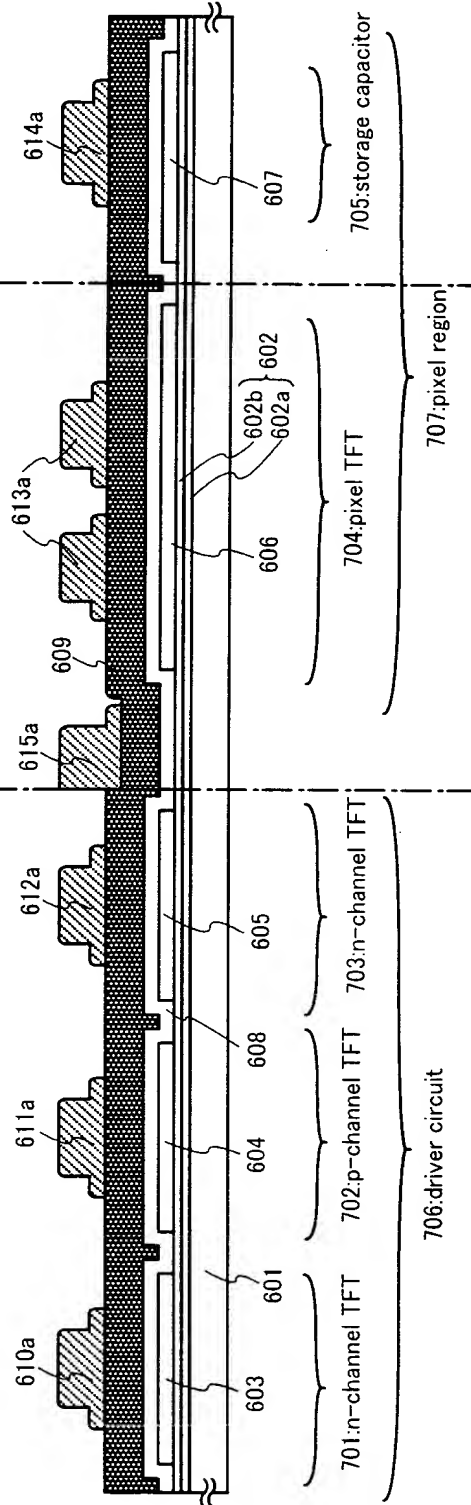


Fig. 6A

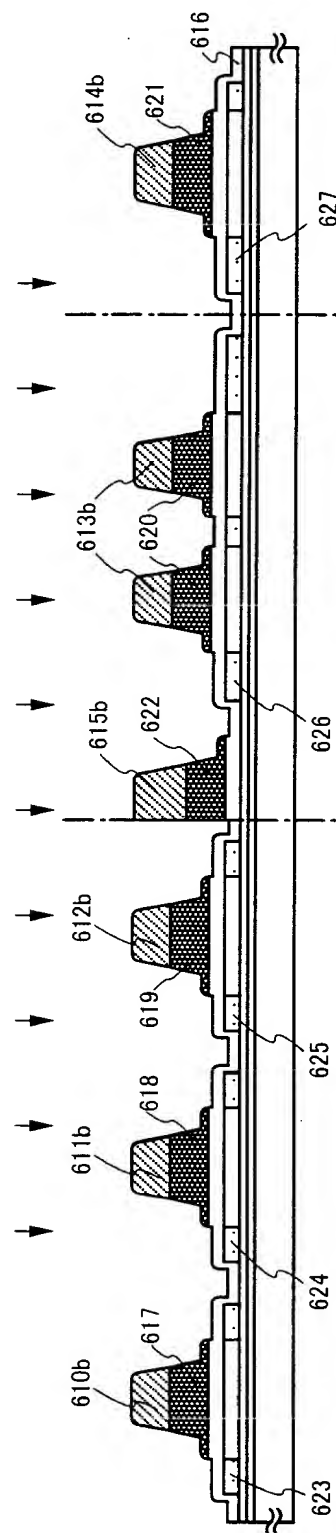


Fig. 6B

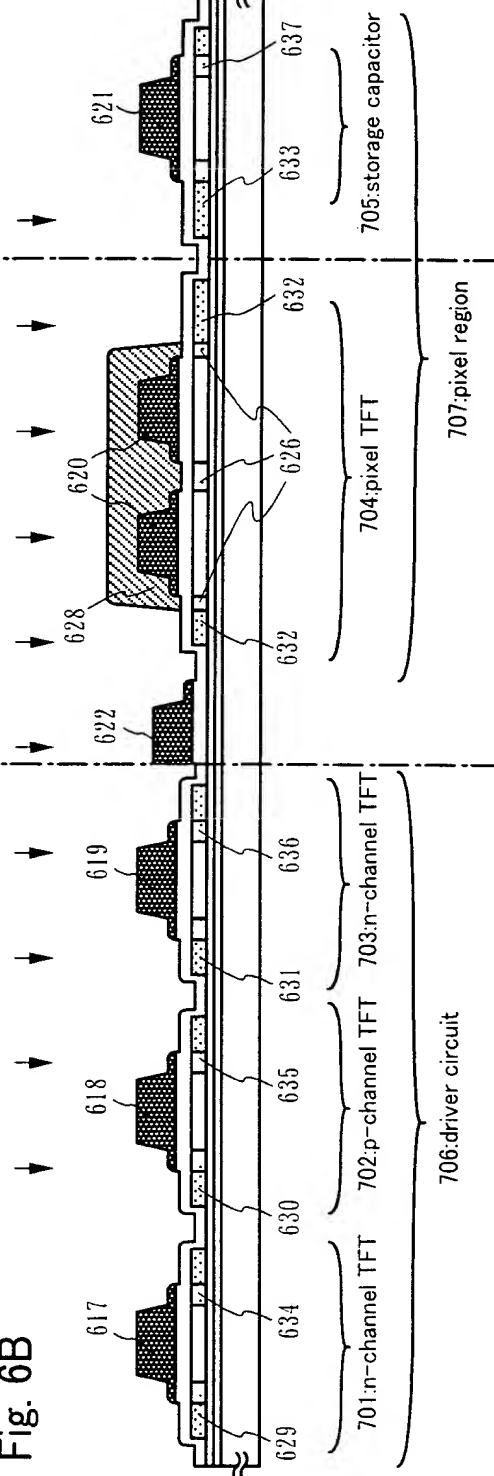


Fig. 7A

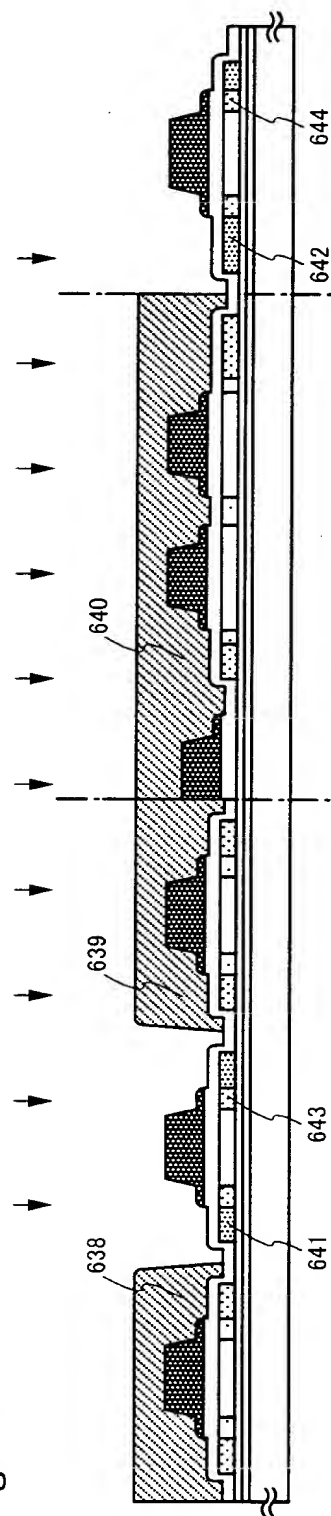


Fig. 7B

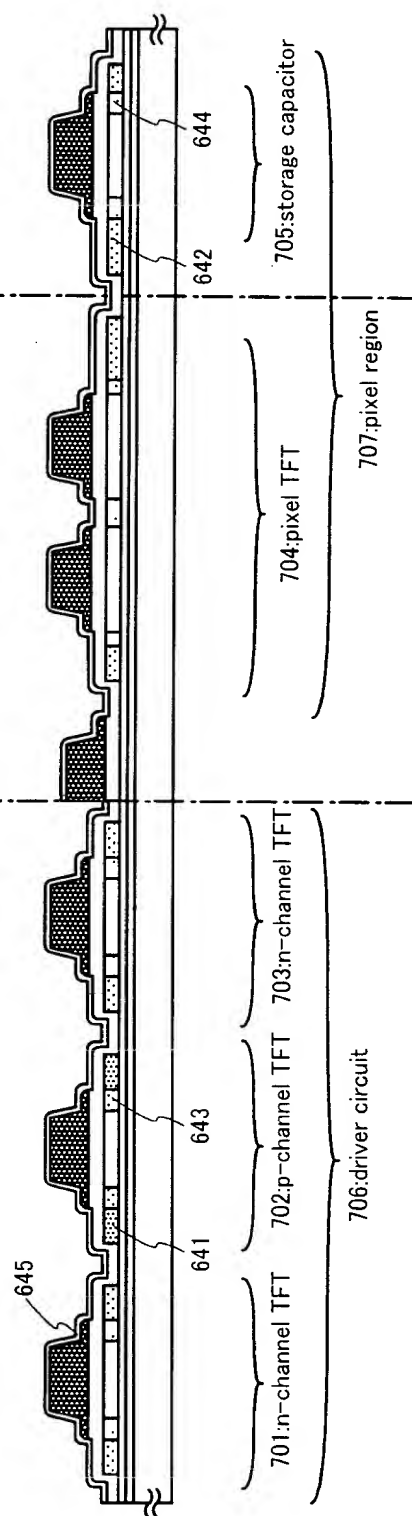


Fig. 8A

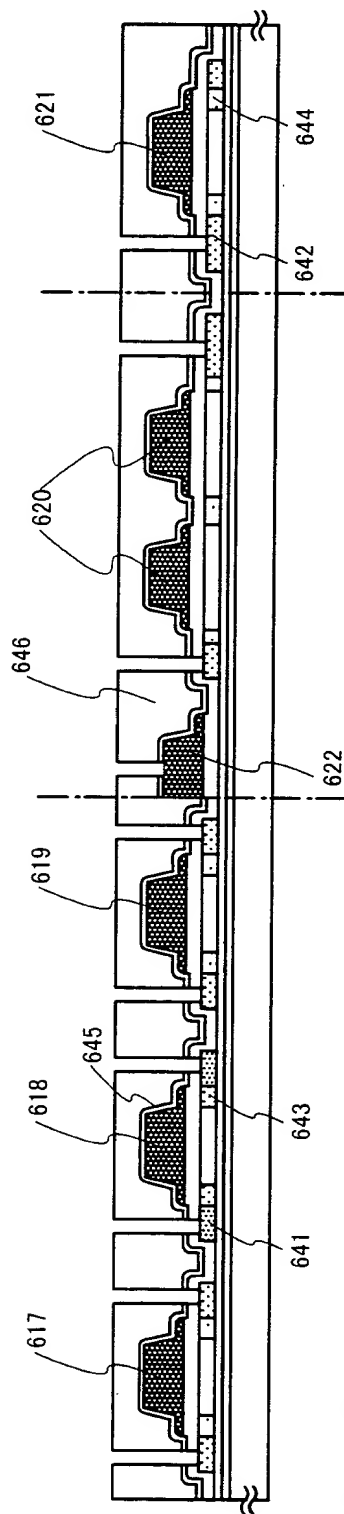


Fig. 8B

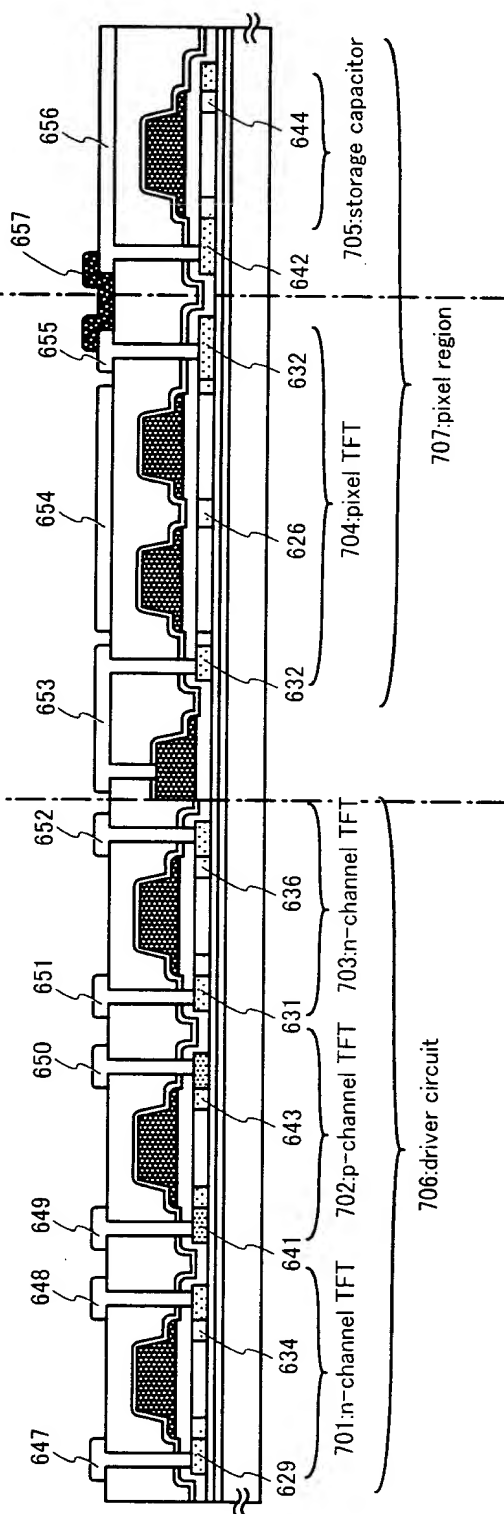


Fig. 9A

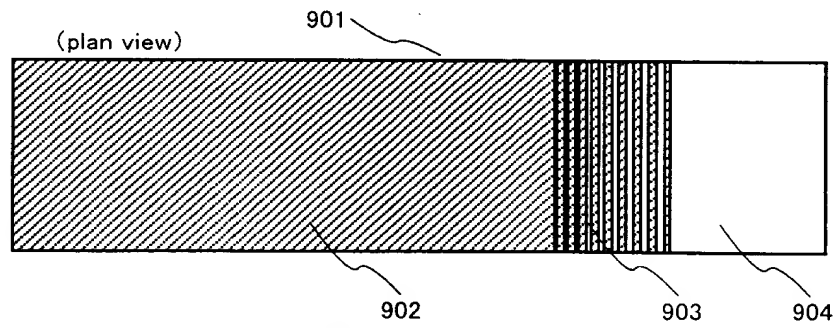


Fig. 9B

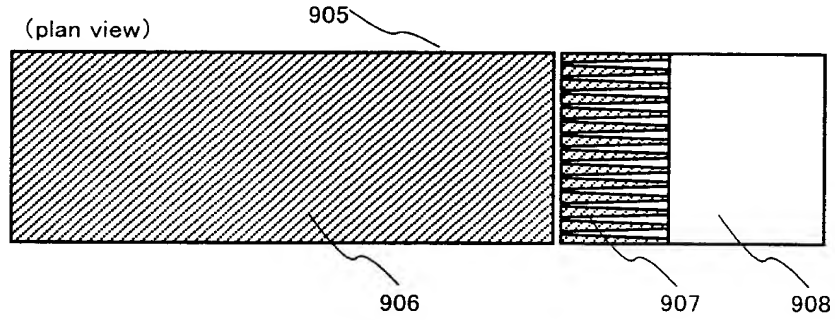


Fig. 9C

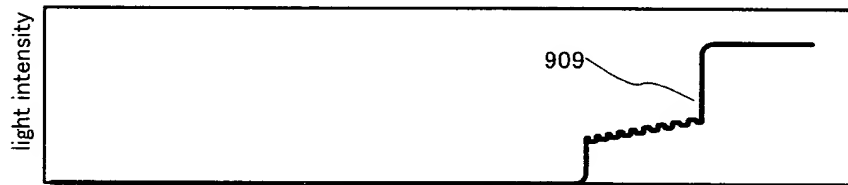


Fig. 9D

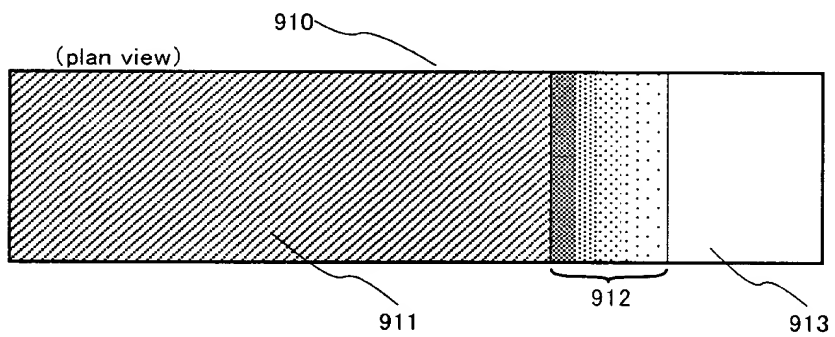


Fig. 9E

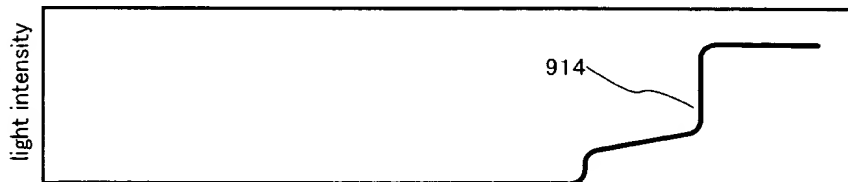


Fig. 10A

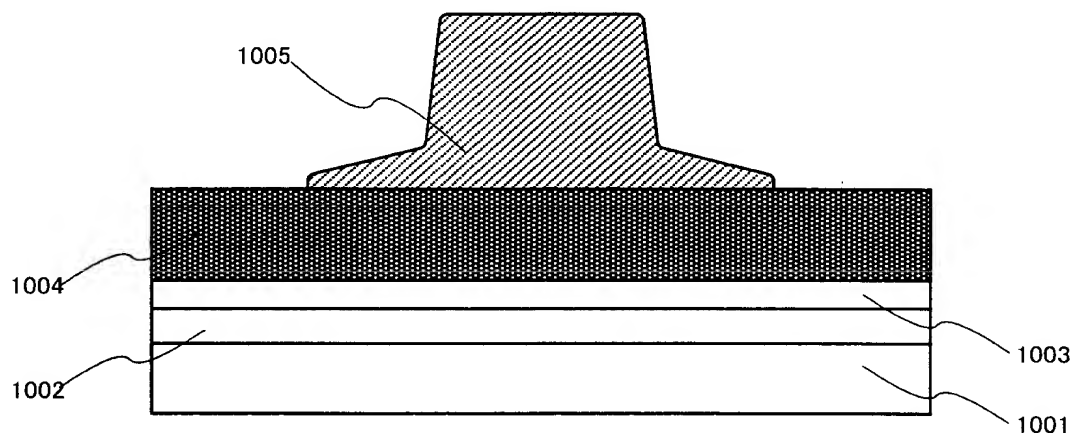


Fig. 10B

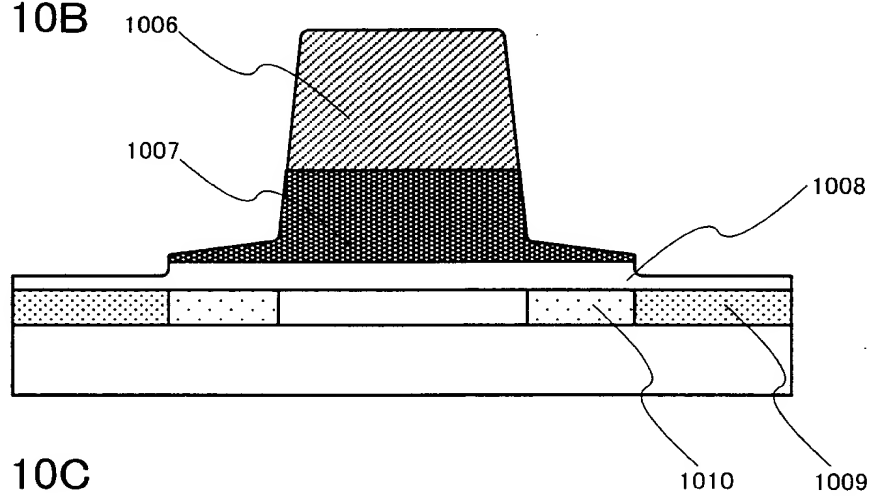


Fig. 10C

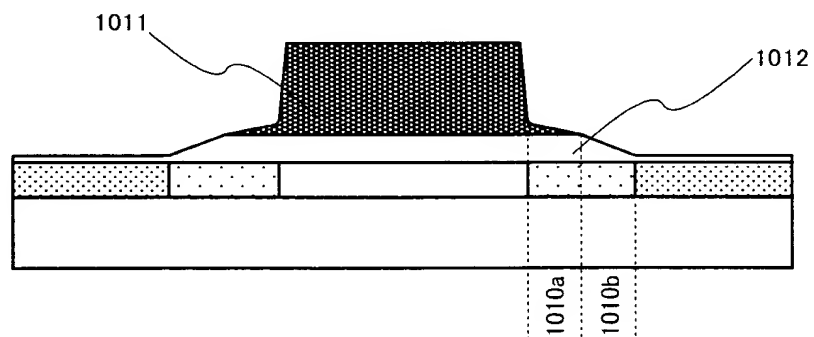


Fig. 11A

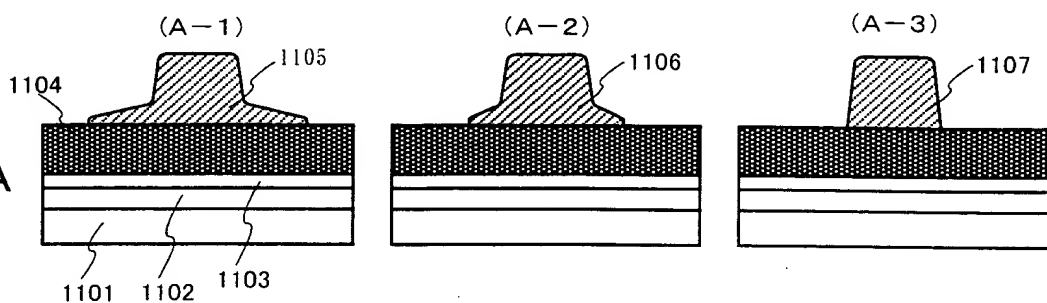


Fig. 11B

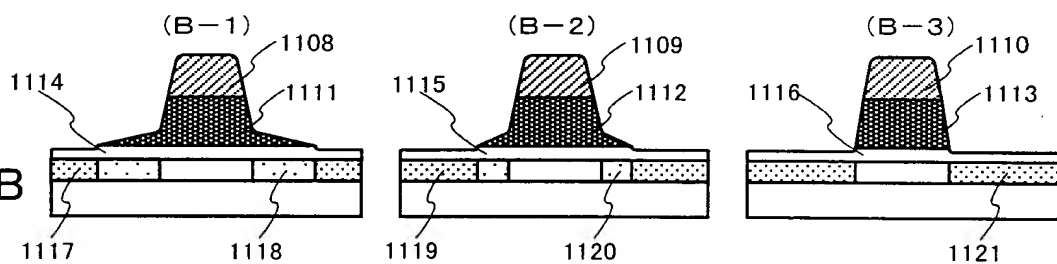


Fig. 11C

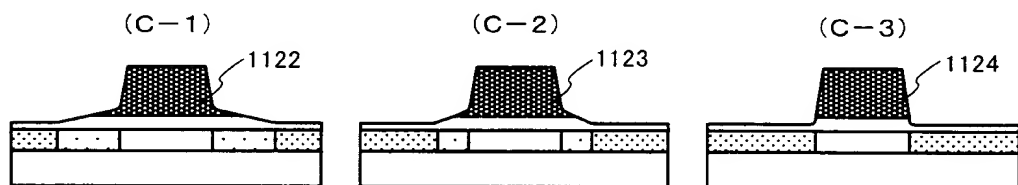


Fig. 11D

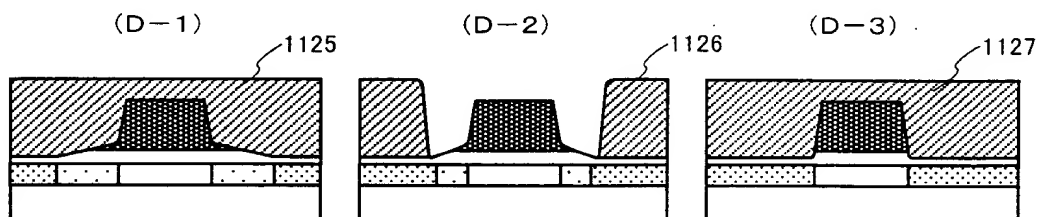


Fig. 11E

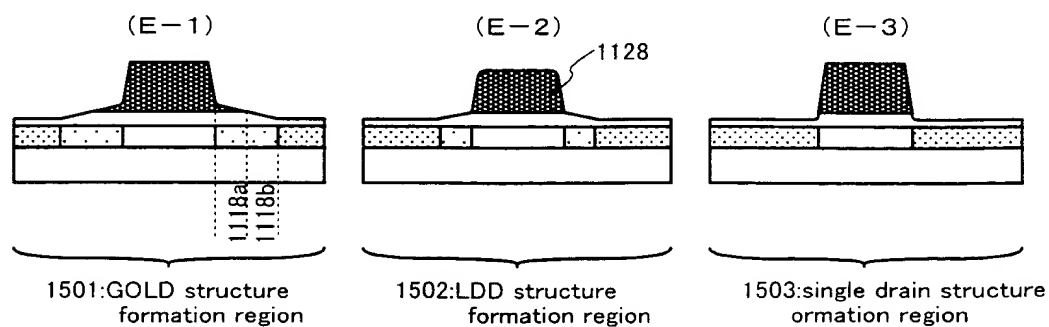


Fig. 12A

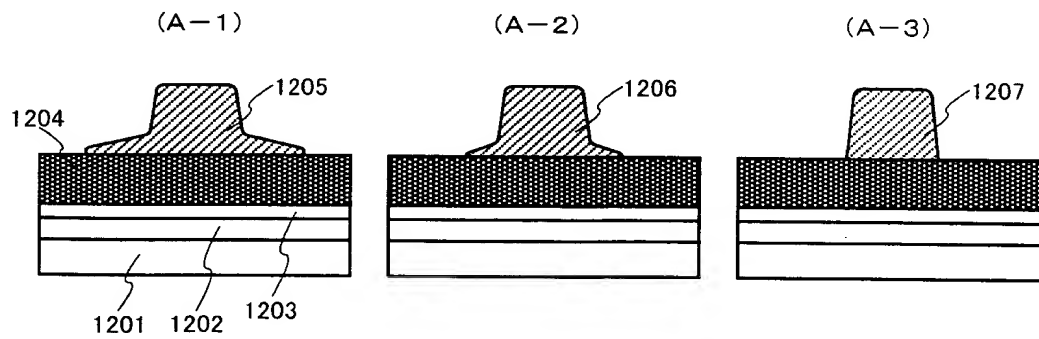


Fig. 12B

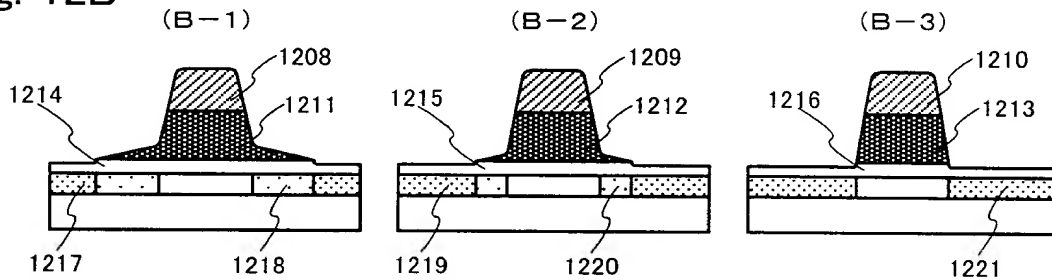


Fig. 12C

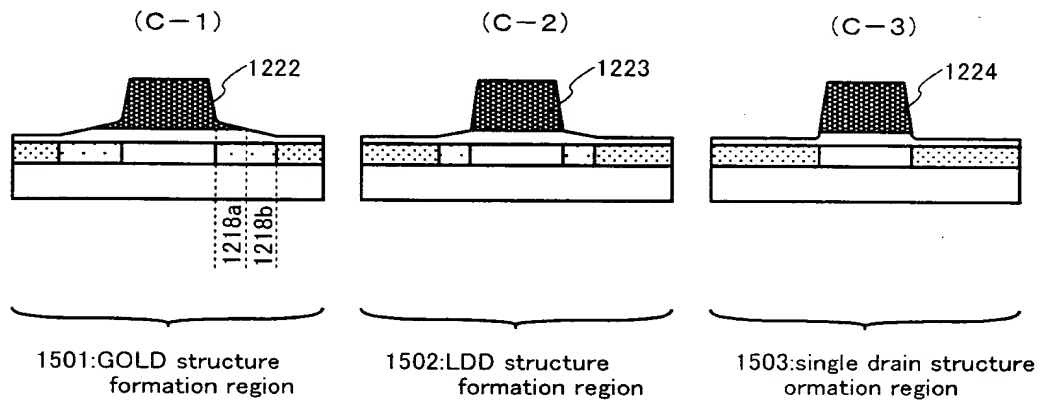


Fig. 13A

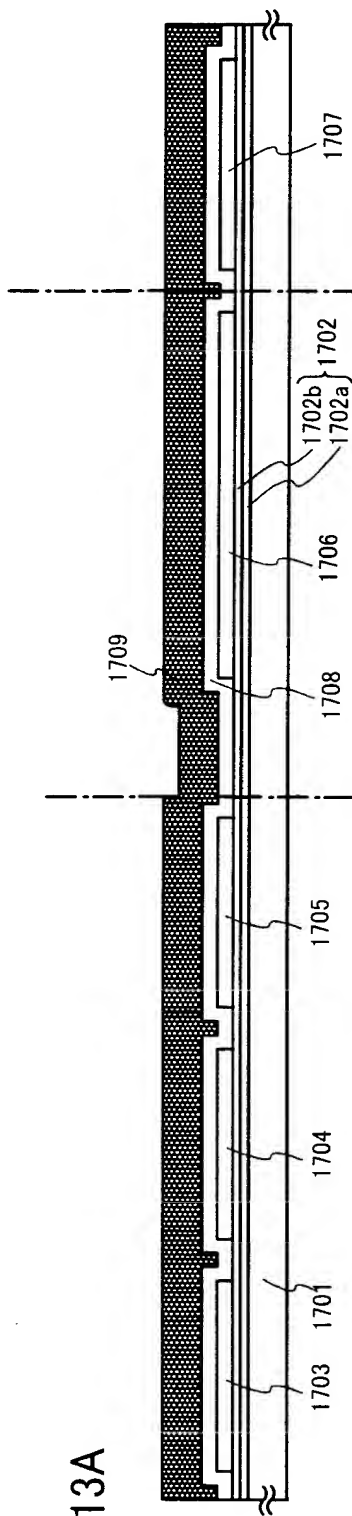


Fig. 13B

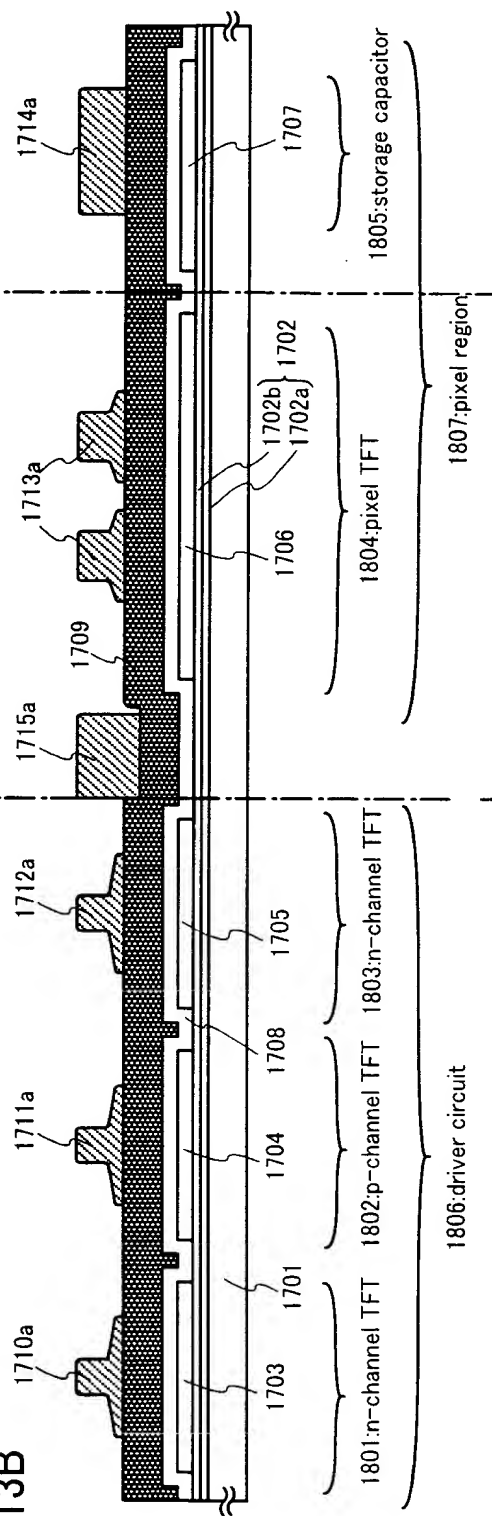


Fig. 14A

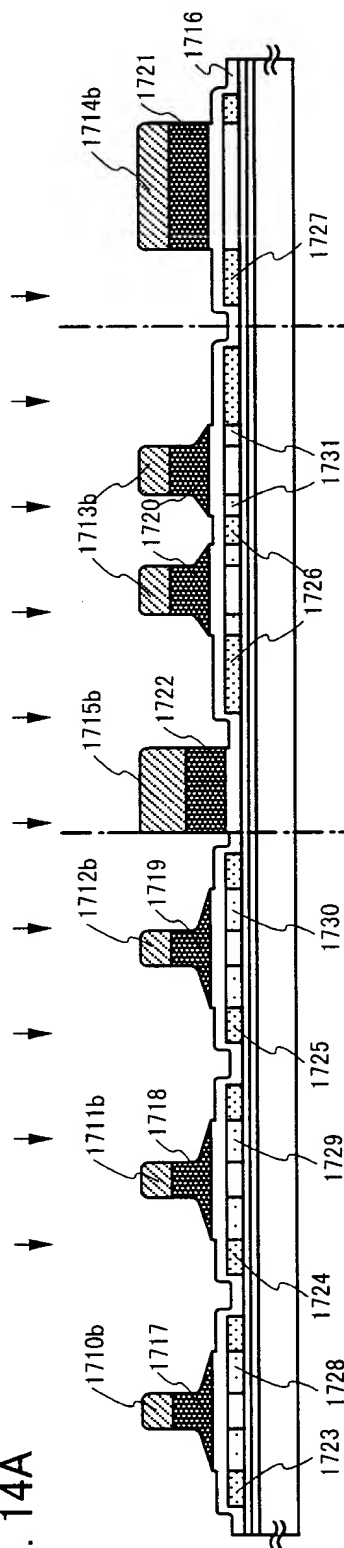


Fig. 14B

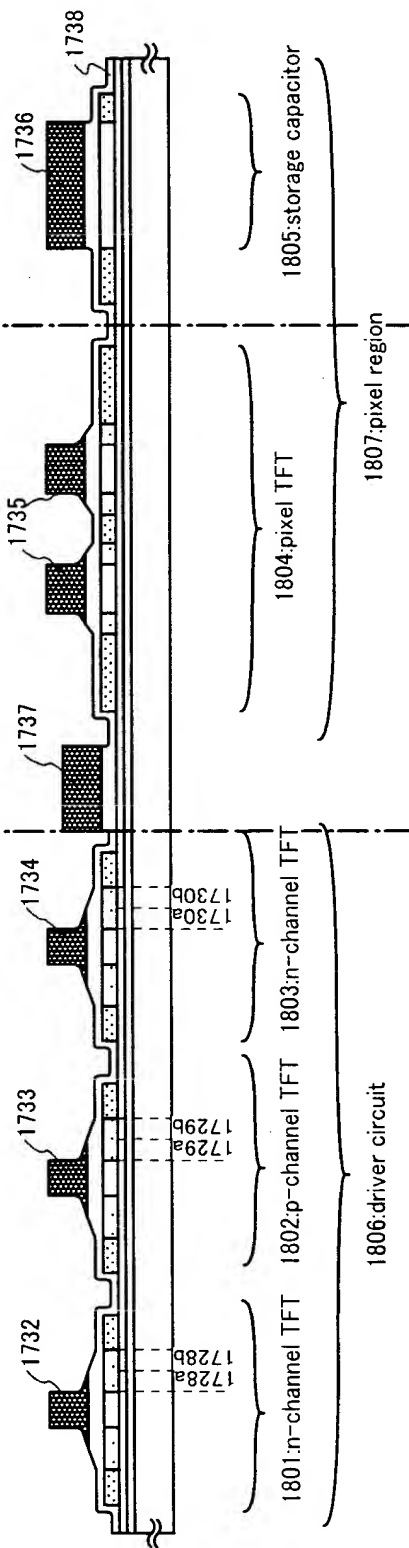


Fig. 15A

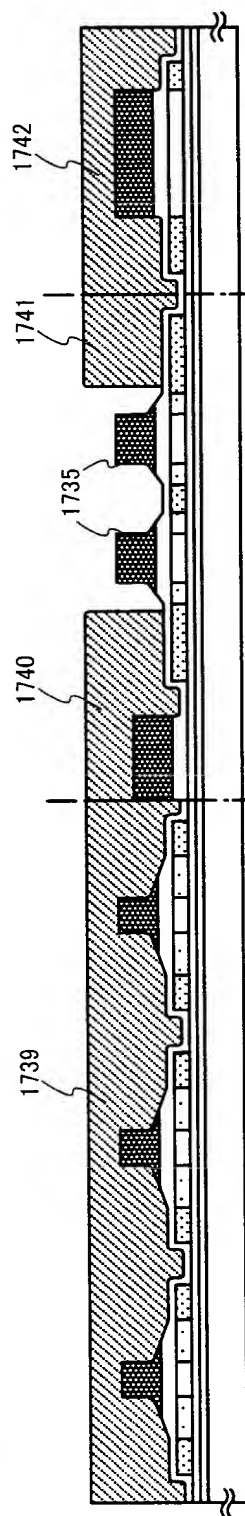


Fig. 15B

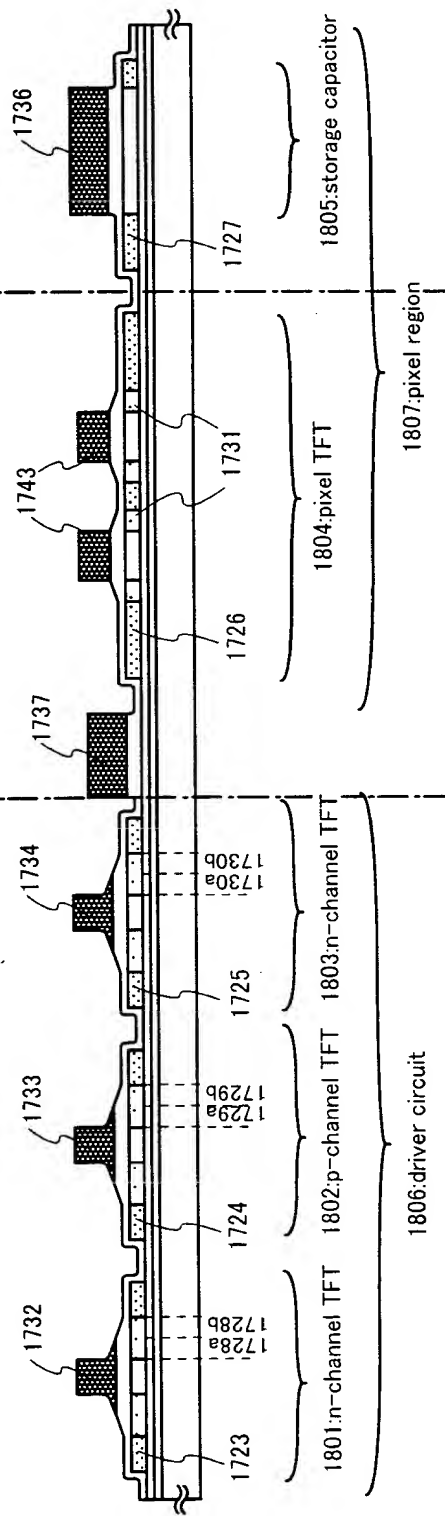


Fig. 16A

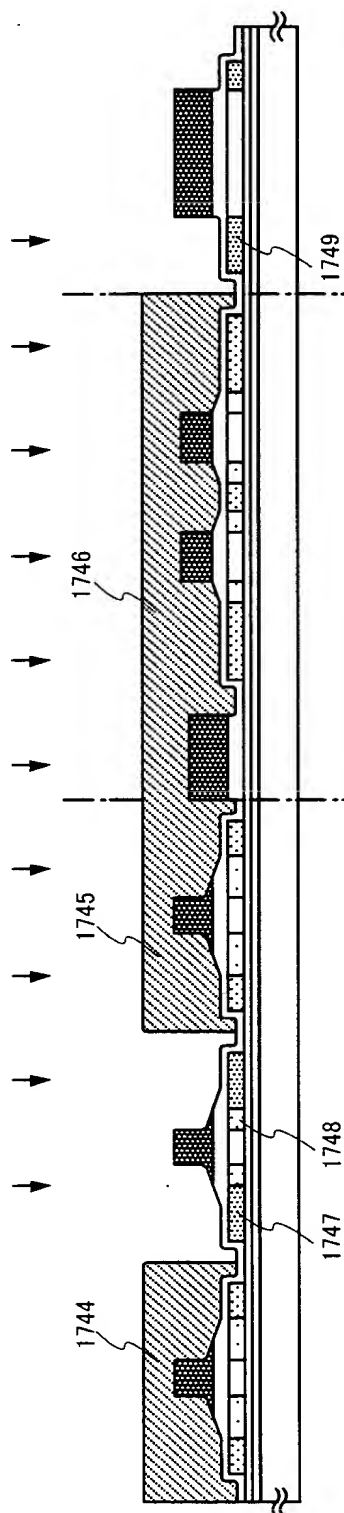


Fig. 16B

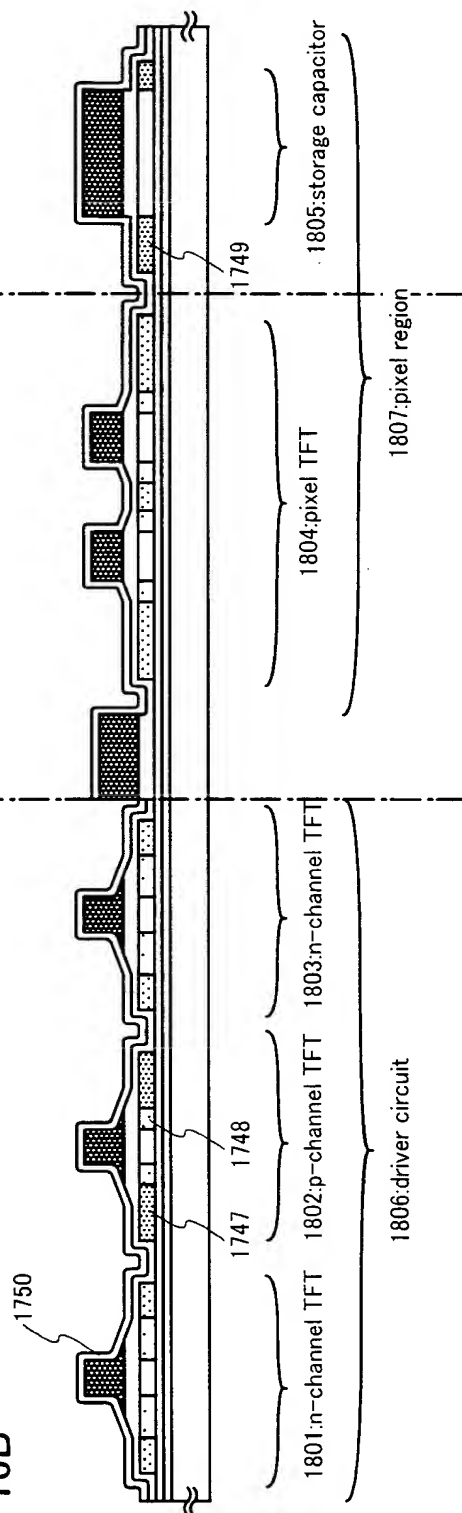


Fig. 17A

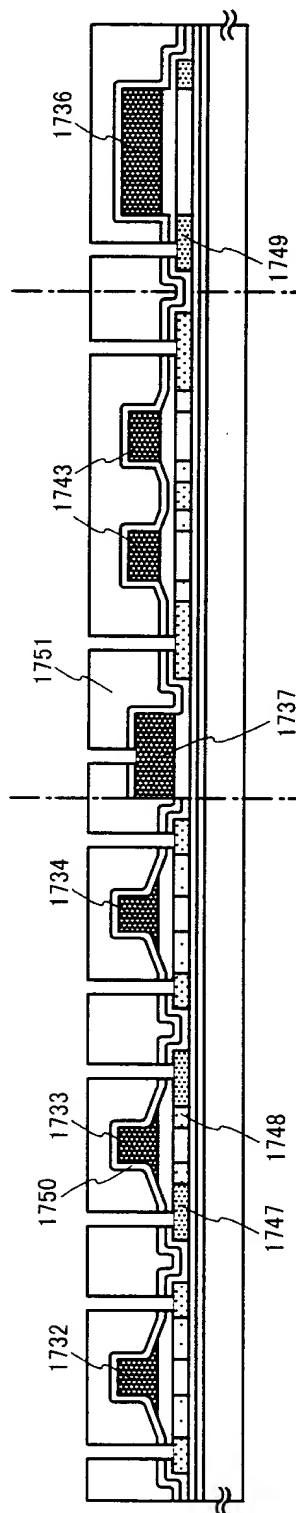
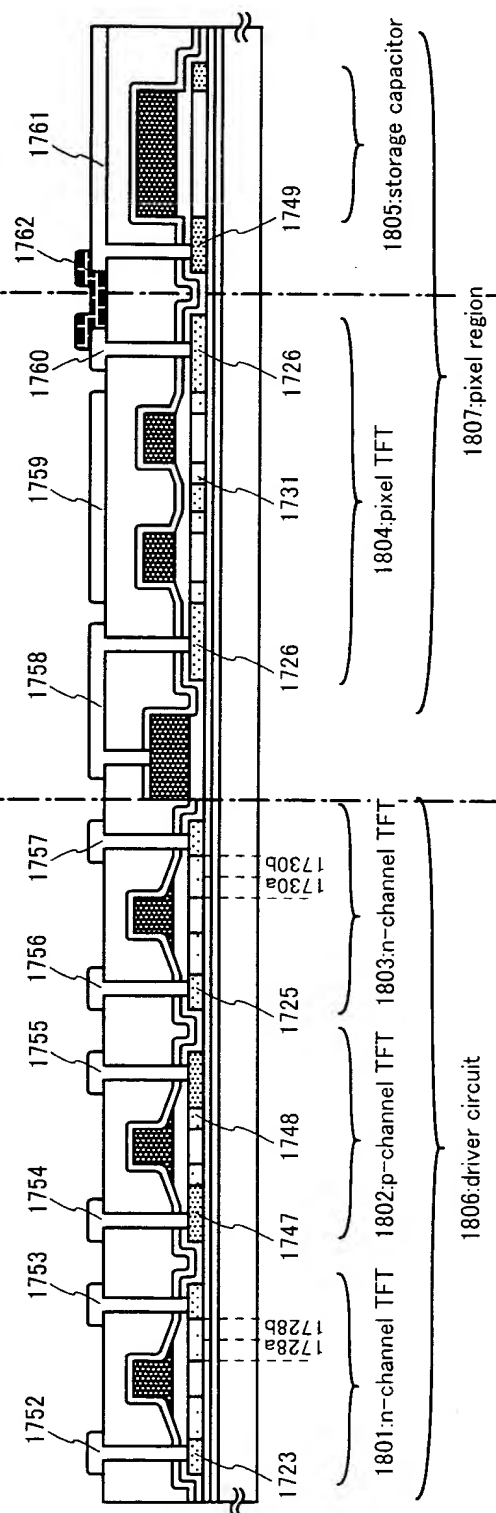


Fig. 17B



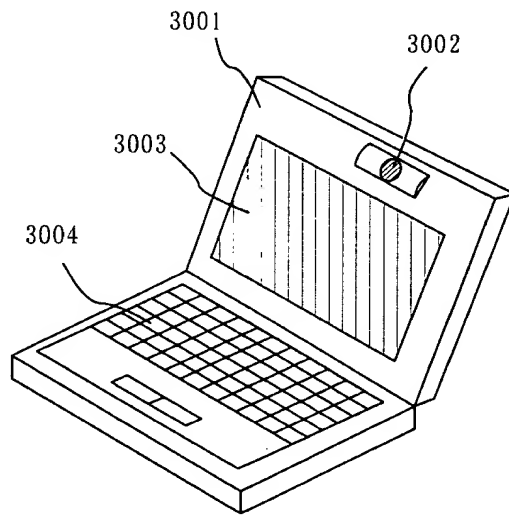


Fig. 18A

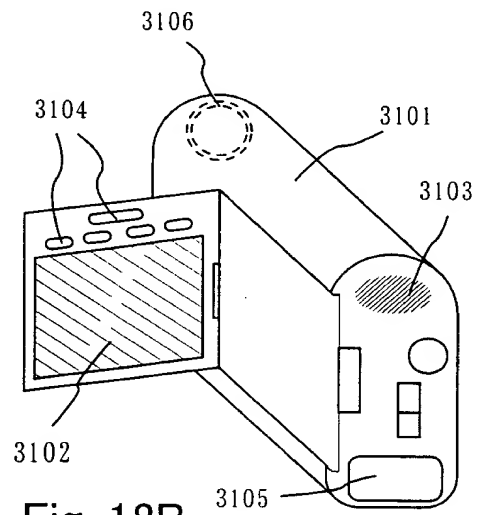


Fig. 18B

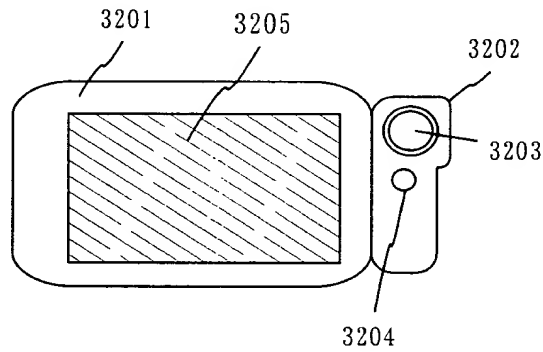


Fig. 18C

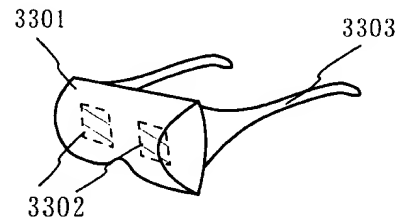


Fig. 18D

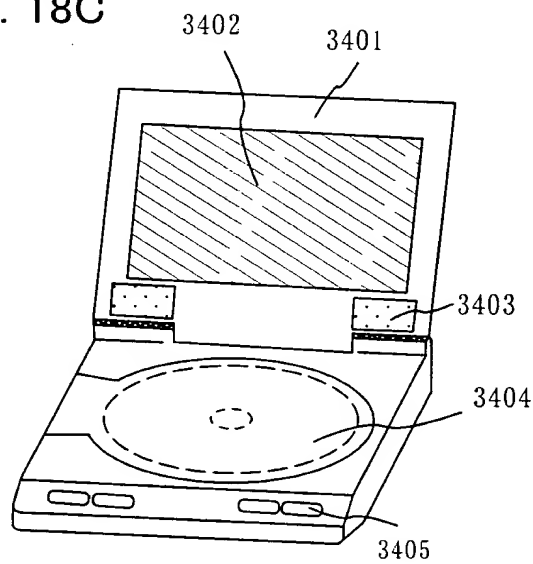


Fig. 18E

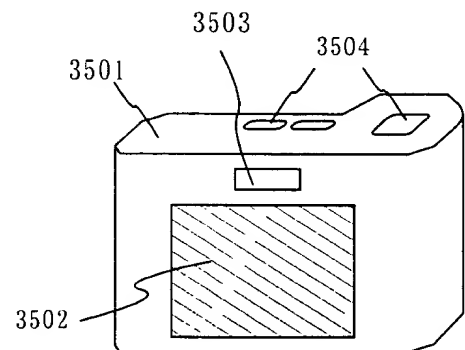


Fig. 18F

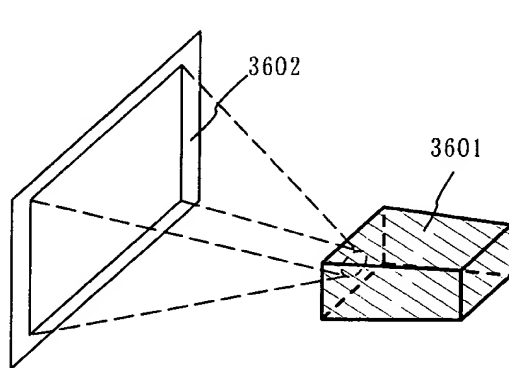


Fig. 19A

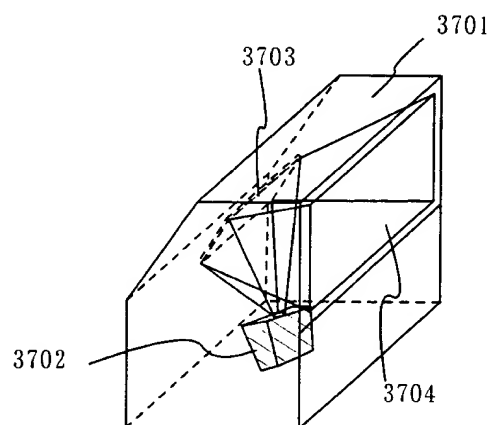


Fig. 19B

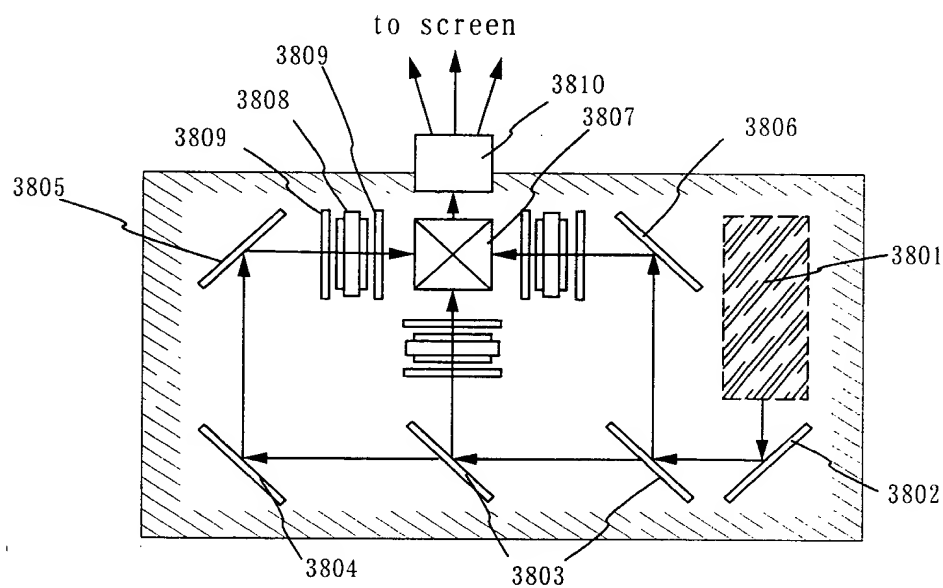


Fig. 19C

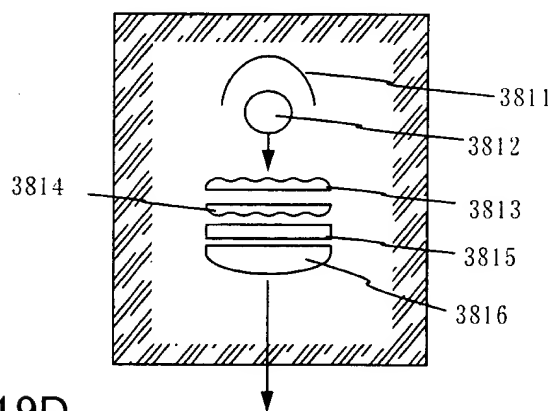


Fig. 19D

Fig. 20A

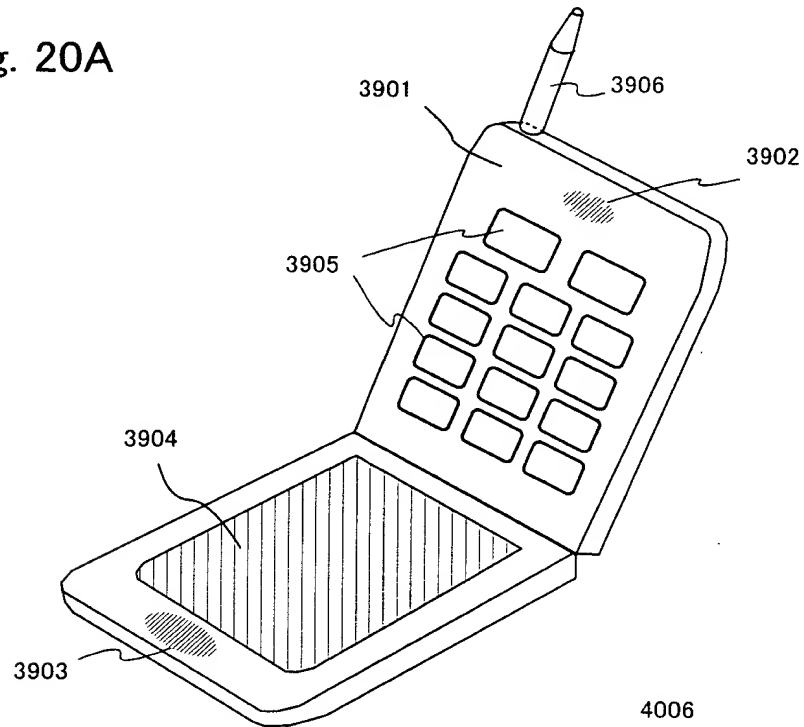


Fig. 20B

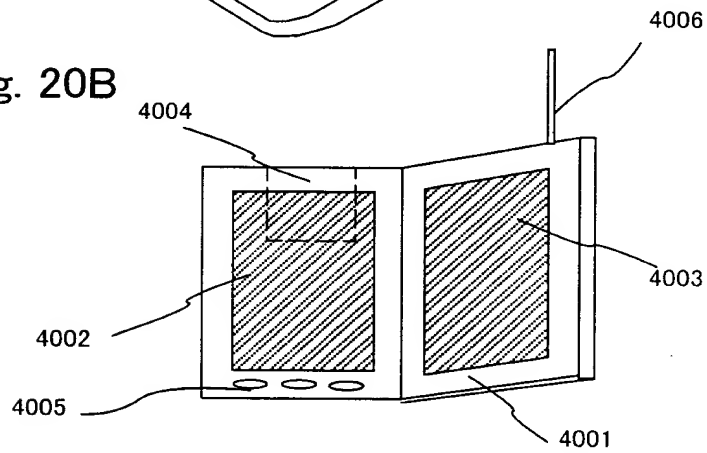


Fig. 20C

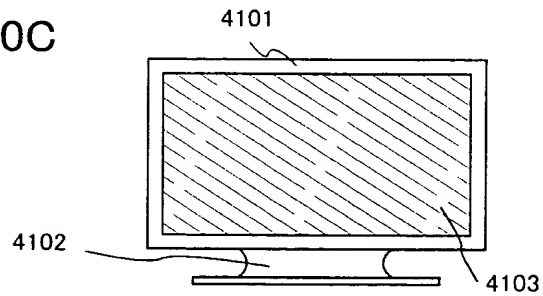


Fig. 21A

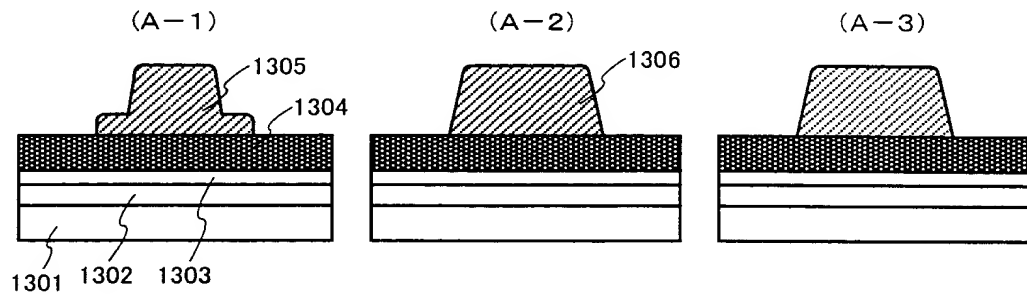


Fig. 21B

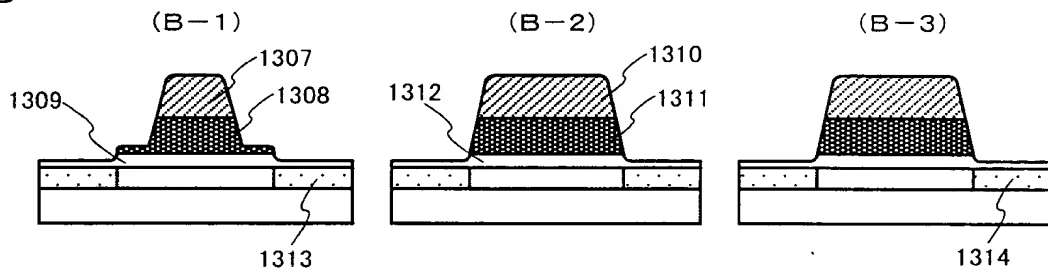


Fig. 21C

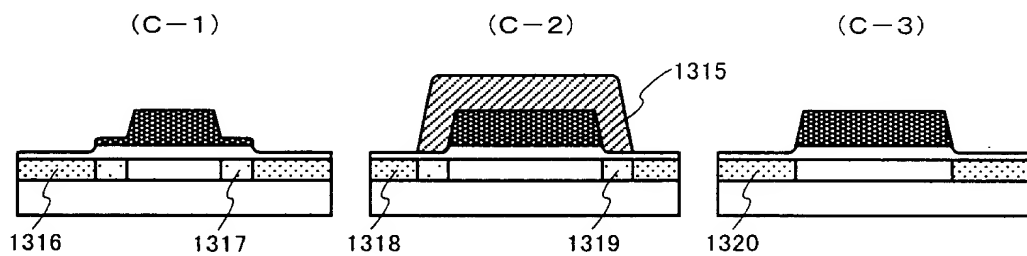


Fig. 21D

